

FIG. 1

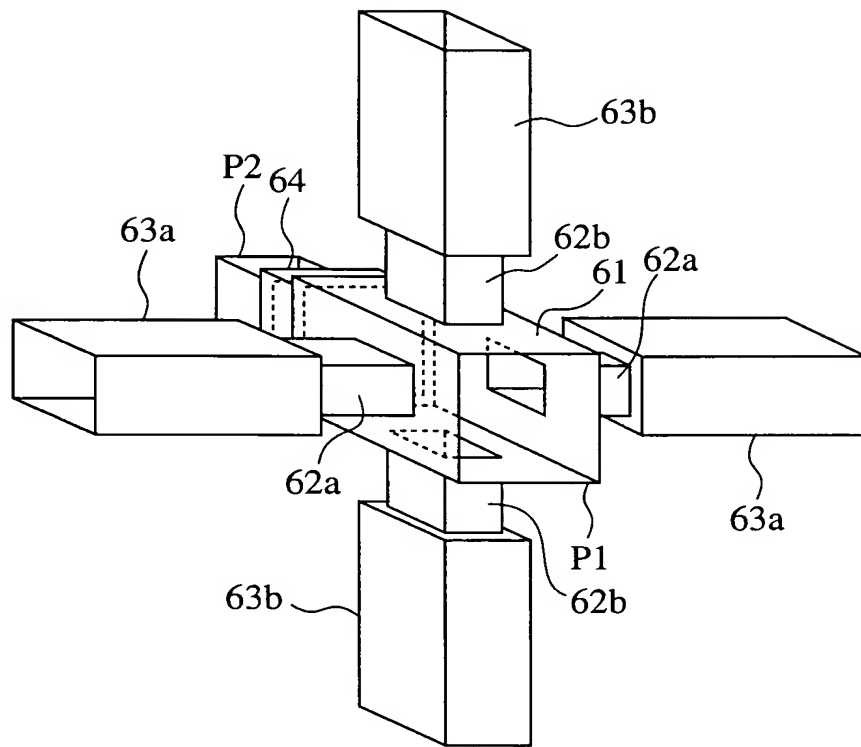
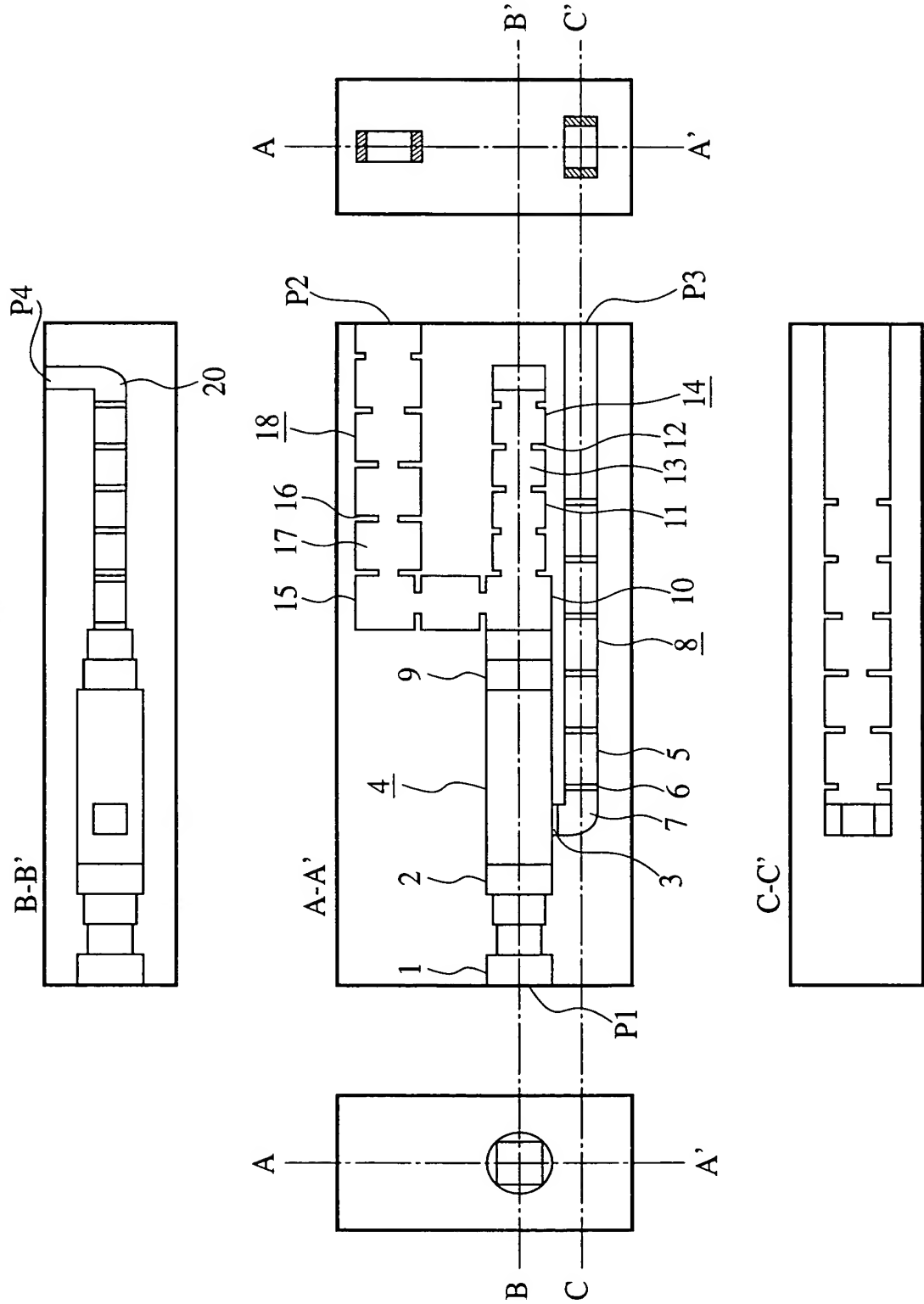


FIG.2



This diagram shows a cross-sectional view of the device along line B-B'. It illustrates the internal structure of the device, including the substrate, the gate stack, the channel region, and the source and drain regions. The gate stack is shown as a series of stacked layers, and the channel region is the central area where the transistor is formed. The source and drain regions are located on either side of the channel. A label 'P4' is shown at the top right, indicating a specific layer or region.

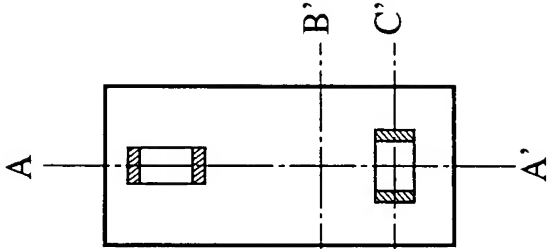
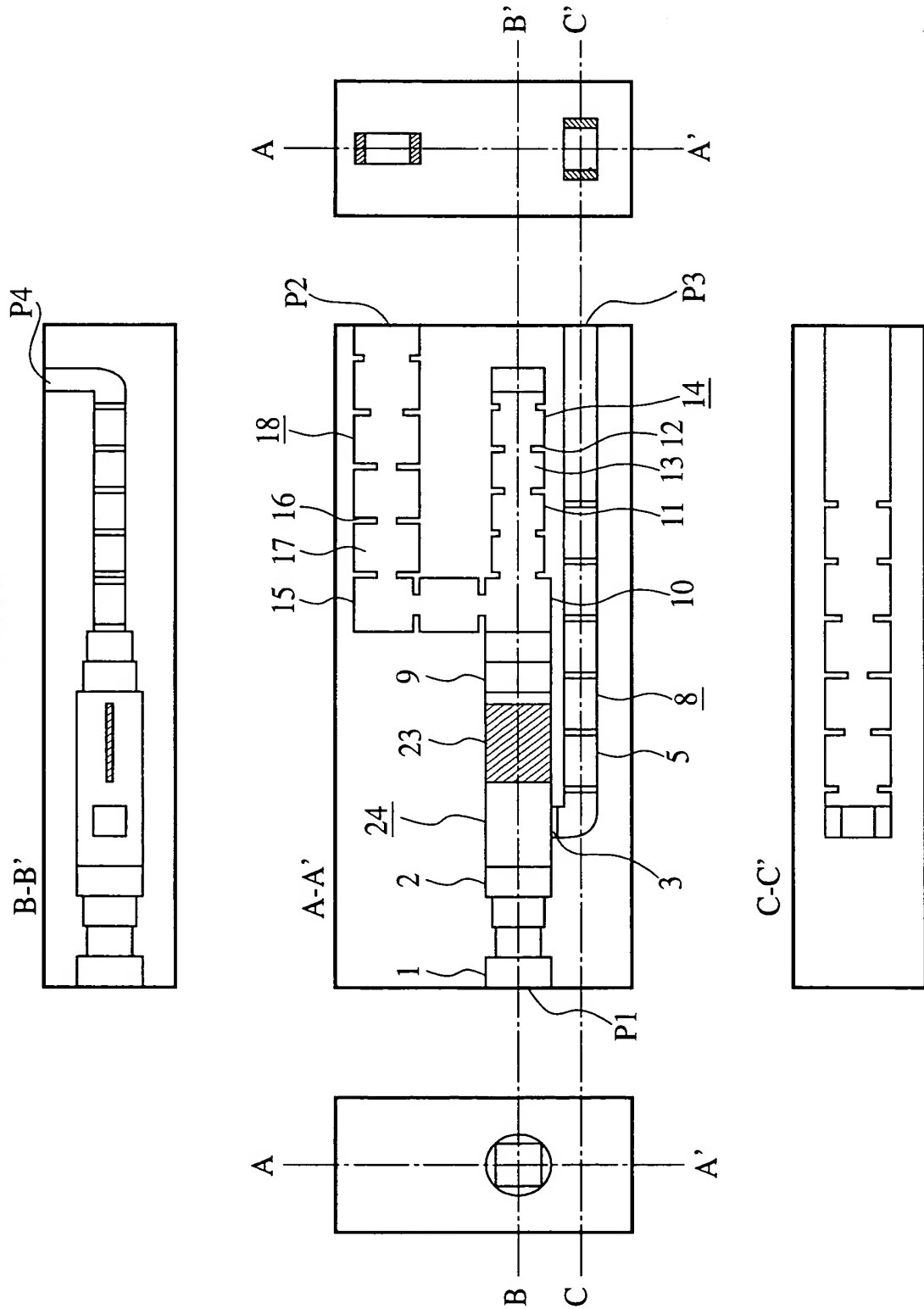


FIG.4



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FIG.5

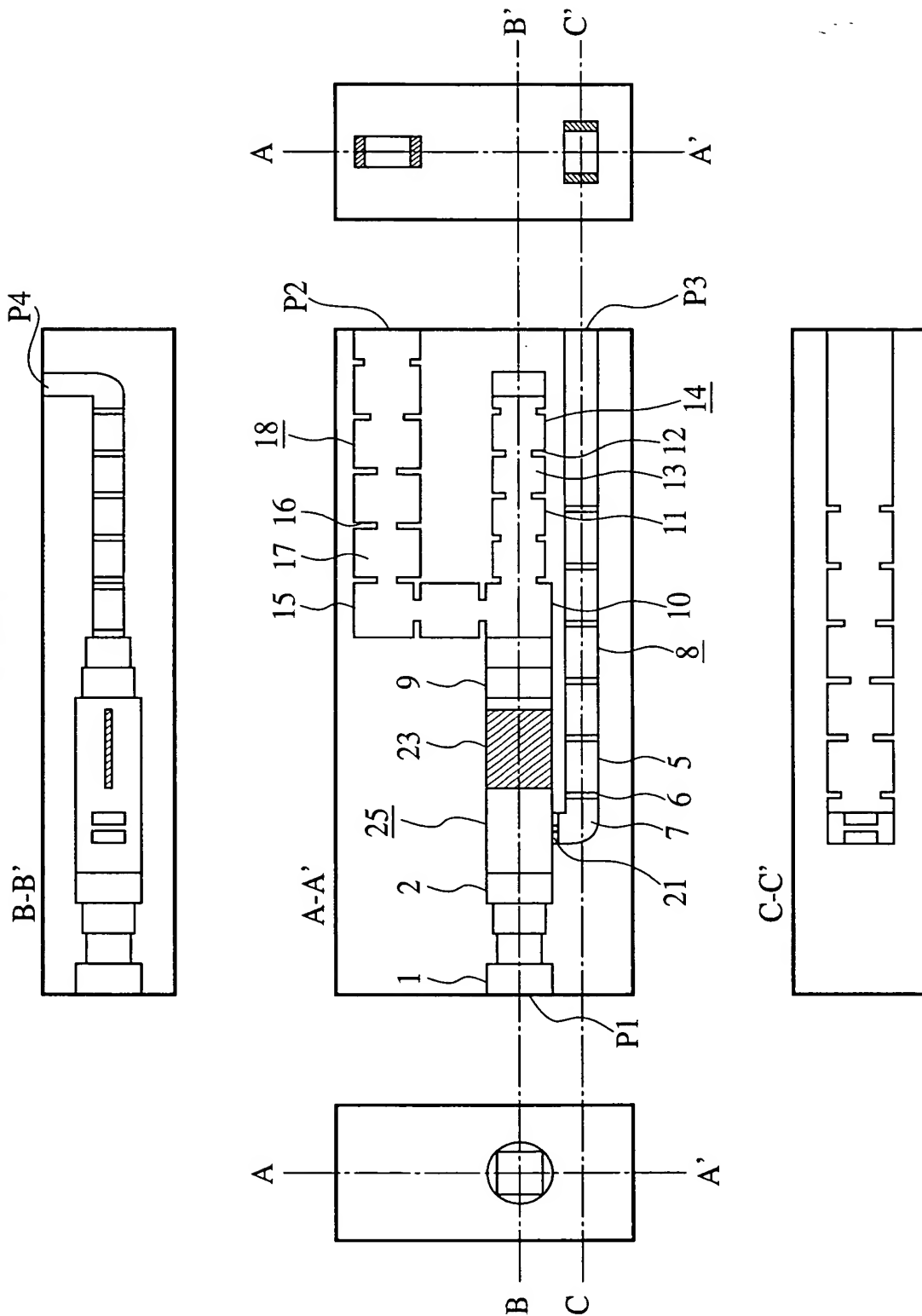


FIG. 6

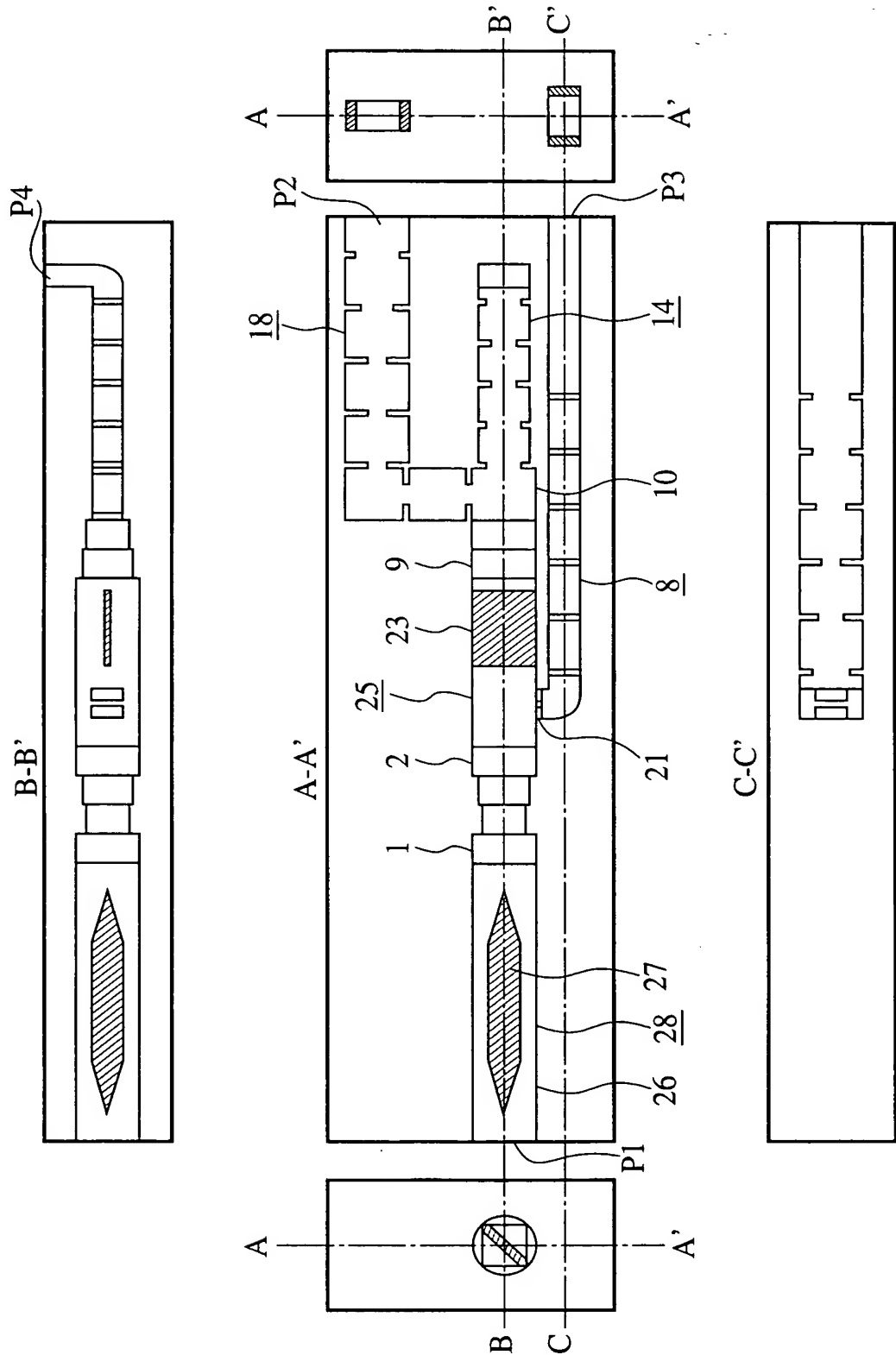


FIG. 7

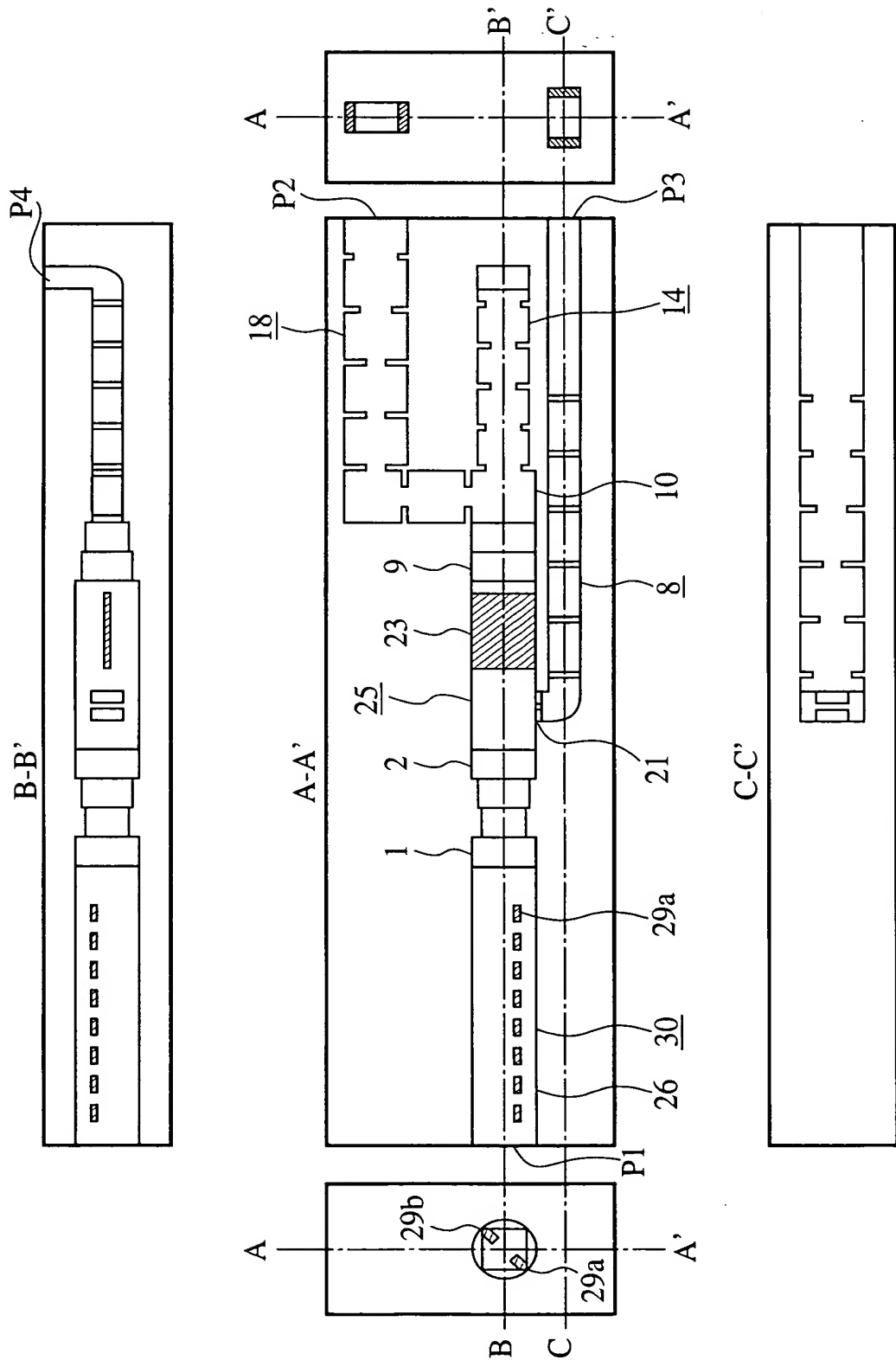


FIG. 8.

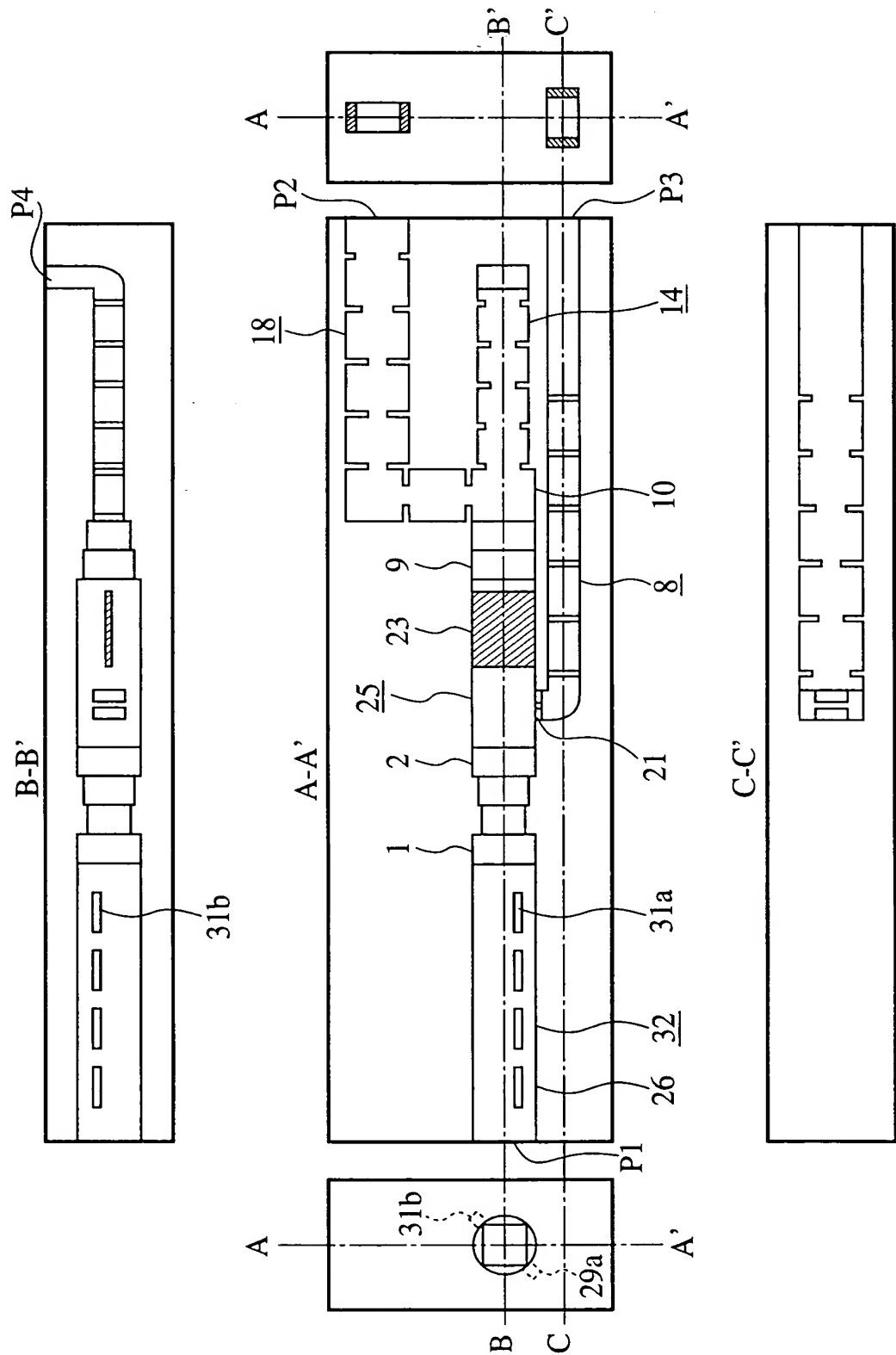
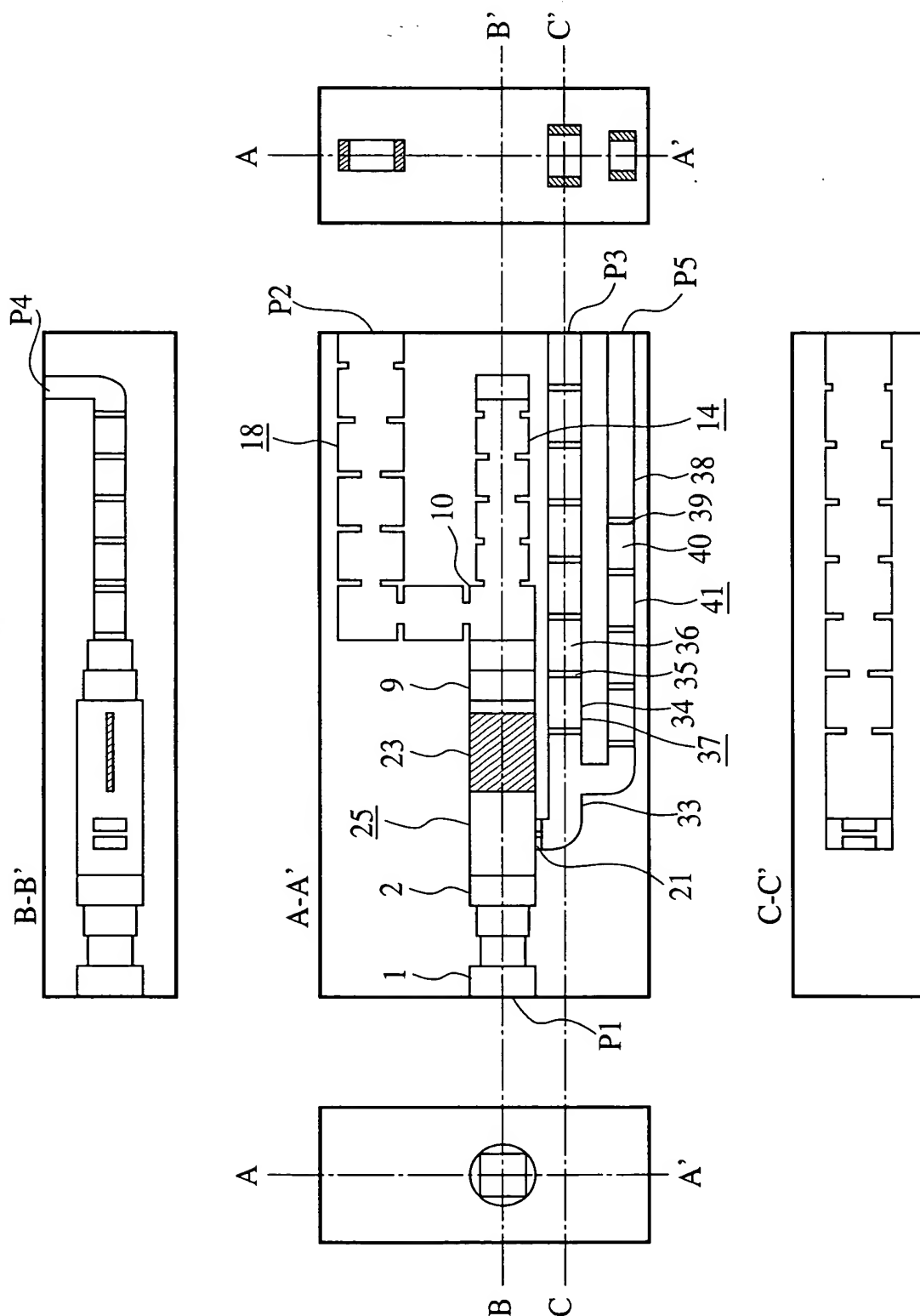


FIG. 9.



This cross-sectional view shows the internal structure of the device. It features a central vertical channel with a hatched pattern. The channel is flanked by two solid blocks. The top of the device is labeled 'P4' with a curved line indicating a specific feature or boundary.

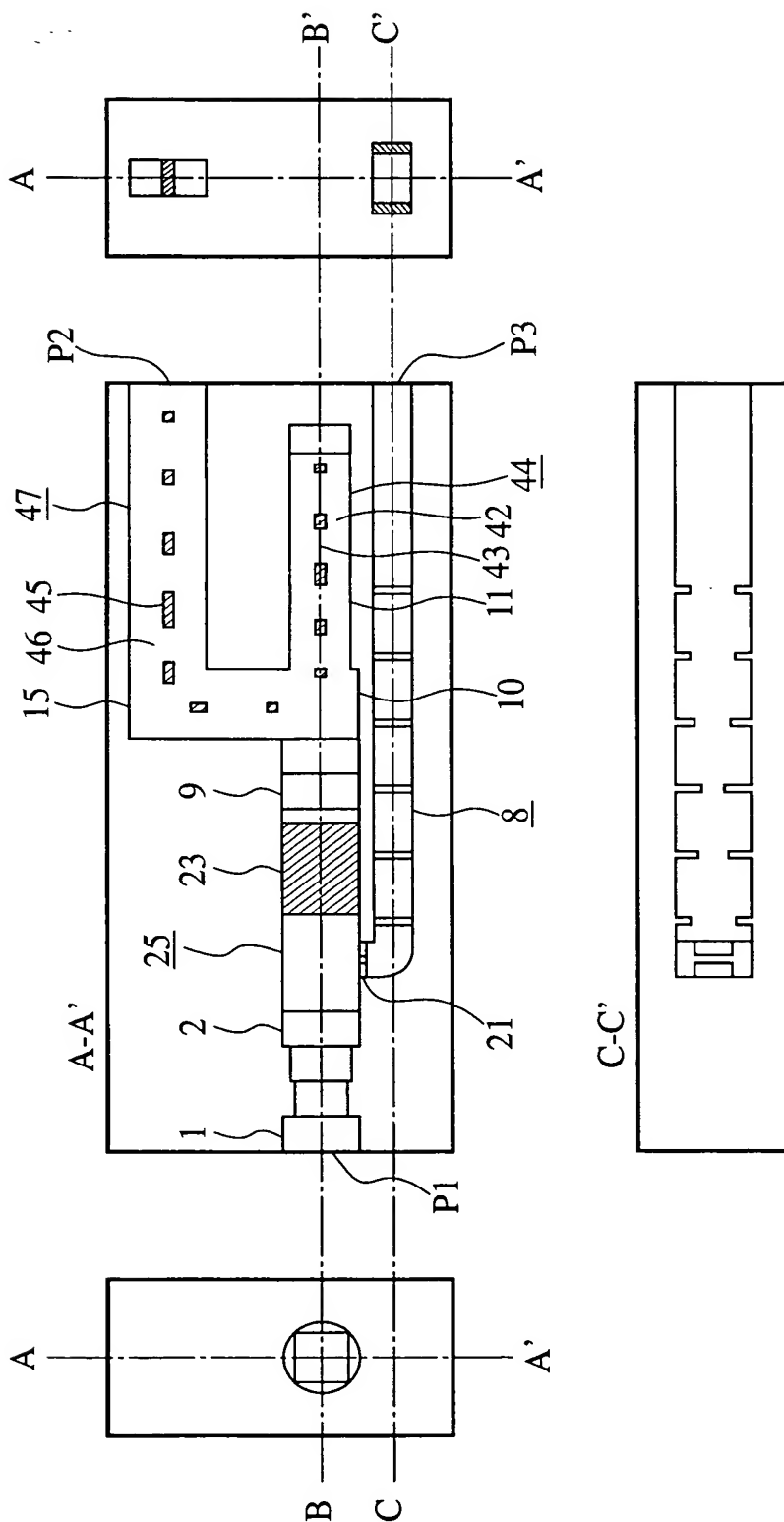
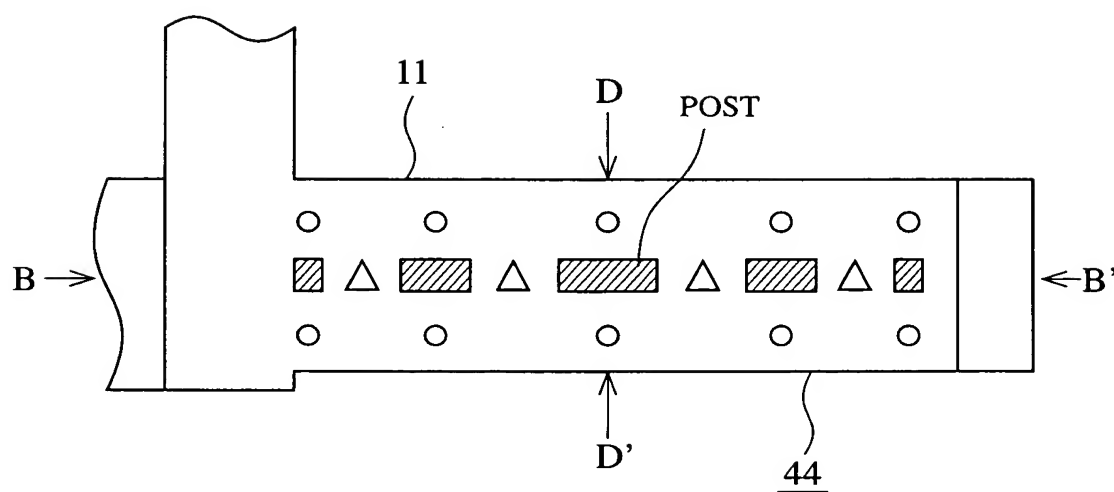
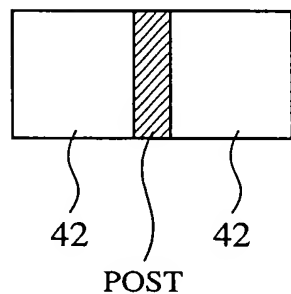


FIG. 11



D-D' CROSS-SECTION



○: POST-TYPE COUPLING HOLES 42
($2m+2=10$)

△: RECTANGULAR CAVITY RESONATORS 43
($m=4$)

FIG. 12

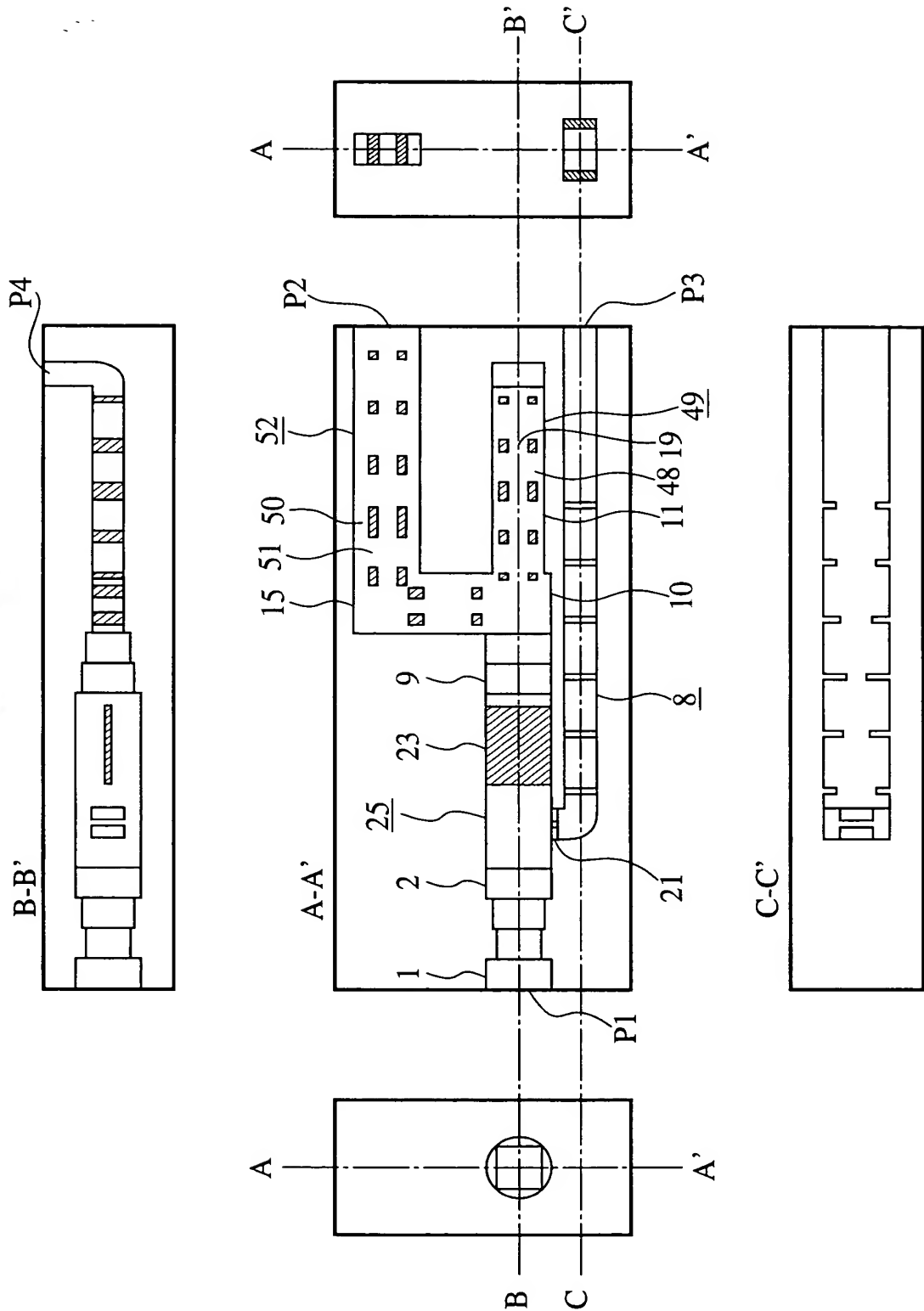
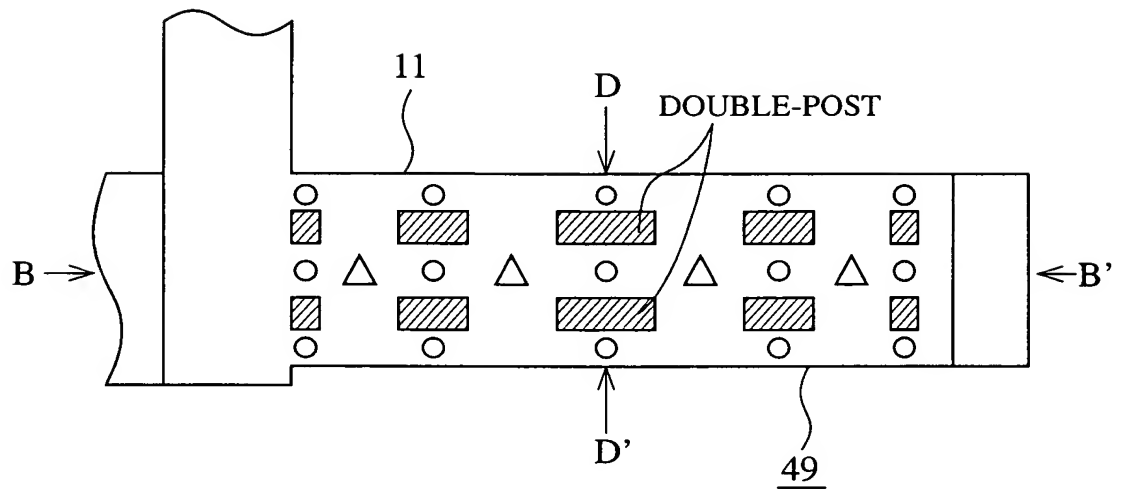
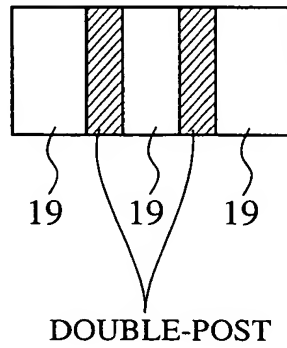


FIG.13



D-D' CROSS-SECTION



○: DOUBLE-POST-TYPE COUPLING HOLES 19
($3m+3=15$)

△: RECTANGULAR CAVITY RESONATORS 48
($m=4$)



FIG.14

